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PATENT APPLICATION  
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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Application No.: 10/813,695 Group: 2416  
Filed: March 29, 2004 Examiner: Kan Yuen  
Confirmation No: 8924  
For: Apparatus and Method for Clock Synchronization in a Multi-Point  
OFDM/DMT Digital Communications System

**PROPOSED AMENDMENT**

42. (Currently Amended) A method for managing a signal, comprising:
- searching for a pilot tone by scanning a frequency range in predetermined frequency steps;
  - recovering a pilot tone sub-symbol;
  - adjusting a frequency offset between the pilot tone and a clock signal to be within a predetermined frequency range as a function of a parameter value difference between the pilot tone sub-symbol and a consecutive pilot tone sub-symbol; and
  - adjusting ~~the~~ a clock signal phase and frequency depending on the parameter value difference to lock on a phase and frequency of the pilot tone.
43. (Previously Presented) The method of Claim 42, wherein recovering the pilot tone sub-symbol comprises adjusting the clock signal frequency so that the pilot tone sub-symbol can be received.
44. (Previously Presented) The method of Claim 42, further comprising identifying the pilot tone sub-symbol.

10/813,695

- 2 -

45. (Previously Presented) The method of Claim 44, wherein identifying the pilot tone sub-symbol comprises scanning a plurality of bins to locate a bin containing the pilot tone sub-symbol.
46. (Currently Amended) The method of Claim 42, wherein the parameter value difference comprises phase.
47. (Previously Presented) The method of Claim 42, further comprising using the clock signal frequency for phase locked loop processing.
48. (Previously Presented) An apparatus for managing a signal, comprising:
- a search unit to search for a pilot tone by scanning a frequency range in predetermined frequency steps;
  - a clock source that recovers a pilot tone sub-symbol;
  - a first adjustment module arranged to adjust a frequency offset between the pilot tone and a clock signal to be within a predetermined frequency range as a function of a parameter value difference between the pilot tone sub-symbol and a consecutive pilot tone sub-symbol; and
  - a second adjustment module to adjust ~~of~~ a signal frequency of the clock source depending on the parameter value difference to lock on a phase and frequency of the clock signal to a phase and frequency of the pilot tone.
49. (Previously Presented) The apparatus of Claim 48, wherein the clock signal source is a voltage controlled oscillator.
50. (Previously Presented) The apparatus of Claim 48, further comprising an identifier of the pilot tone sub-symbol.

10/813,695

- 3 -

51. (Currently Amended) The apparatus of Claim 48, wherein the parameter value difference comprises phase.
52. (Previously Presented) The apparatus of Claim 48, further comprising a phase locked loop processor that processes based on the signal frequency.
53. (Previously Presented) The method of Claim 42 further including locking on the phase and frequency of the pilot tone as a function of adjusting a voltage controlled oscillator using a phase locked loop.
54. (Previously Presented) The apparatus of Claim 48 further including a locking module arranged to lock on the phase and frequency of the pilot tone as a function of adjusting a voltage controlled oscillator using a phase locked loop.
55. (Currently Amended) ~~A computer-readable medium having computer-readable program codes embodied therein~~ An apparatus for managing a signal, the ~~computer-readable-medium program codes including instructions that, when executed by a processor, cause the processor to~~ apparatus comprising:
- means for search searching for a pilot tone by scanning a frequency range in predetermined frequency steps;
  - means for recover recovering a pilot tone sub-symbol;
  - means for adjust adjusting a frequency offset between the pilot tone and a clock signal to be within a predetermined frequency range as a function of a parameter value difference between the pilot tone sub-symbol and a consecutive pilot tone sub-symbol; and
  - means for adjust adjusting the a clock signal phase and frequency depending on the parameter value difference to lock on a phase and frequency of the pilot tone.
56. (Currently Amended) The ~~computer-readable-medium~~ apparatus of Claim 55 wherein the ~~instructions-cause the processor~~ means for recovering is arranged to recover the pilot tone

10/813,695

- 4 -

sub-symbol as a function of adjusting the clock signal frequency so that the pilot tone sub-symbol can be received.

57. (Currently Amended) The ~~computer-readable-medium~~ apparatus of Claim 55 instructions ~~cause the processor further including means for identify~~ identifying the pilot tone sub-symbol.

58. (Currently Amended) The ~~computer-readable-medium~~ apparatus of Claim 55 instructions ~~cause the processor further including means for to-identify~~ identifying the pilot tone sub-symbol as a function of scanning a plurality of bins to locate a bin containing the pilot tone sub-symbol.

59. (Currently Amended) The ~~computer-readable-medium~~ apparatus of Claim 55 wherein the parameter value difference comprises phase.

60. (Currently Amended) The ~~computer-readable-medium~~ apparatus of Claim 55 wherein the instructions ~~cause the processor means for adjusting clock phase and frequency~~ use the clock signal frequency for phase locked loop processing.

61. (Currently Amended) The ~~computer-readable-medium~~ apparatus of Claim 55 wherein the instructions ~~cause the processor means for adjusting clock phase and frequency is arranged~~ to lock on the phase and frequency of the pilot tone as a function of adjusting a voltage controlled oscillator using a phase locked loop.